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David I. J. Glen

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ADVANCED MICRO DEVICES, INC.

C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.

222 N.LASALLE STREET

CHICAGO, IL 60601

EXAMINER

AMINI, JAVID A

ART UNIT

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2628

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/484,123

Applicant(s)

GLEN, DAVID I. J.

Examiner

Javid A. Amini

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 June 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) 5,13,15,22 and 24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,6-12,14,16-21,23 and 25-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/7/2007 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4, 6-12, 14, 16-21, 23, 25-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1-4, 6-12, 14, 16-21, 23, 25-33 contain terms e.g., "operable to" "operably" and "operatively", the Examiner believes the terms "operable", "operably" and "operatively" render the claims indefinite. Because the terms provide the possibility of the operation in the claimed invention, the terms are not considered definite. An ordinary skill in the art can not be determined the subject matter, because the subject matter is lacking precise limits, another words the subject matter is undecided, e.g., a lot of thing is possible but it is uncertain to obtain a result.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6-12, 14, 16-21, 23, 25-33 are rejected under 35 U.S.C. 102(e) as being anticipated by MacInnis et al. US 6,501,480 B1 (hereinafter refers as a MacInnis).

1. Claim 1.

As for claim 1, “A video graphics module (MacInnis in fig. 1 illustrates it) comprises: a plurality of video graphics pipelines (MacInnis in fig. 4 illustrates a graphic pipeline as 80 and a video pipeline as 82 which both are considered as video graphics pipelines. Furthermore, cols. 43-44, lines 63 and 7, respectively, suggests a plurality of video graphics pipeline.), wherein each of the plurality of video graphics pipelines is operable to process a corresponding image layer and wherein one of the plurality of video graphics pipelines processes a foremost **graphics** image layer and the video (MacInnis in col. 1 lines 54-60 discloses that both the functionality of the graphics and video are common to both. Graphics as used herein may include graphics, text, and video) **graphics pipelines is operable to process** the corresponding image layers in parallel (MacInnis at col. 45 lines 10-11 teaches in an alternate embodiment, two or more of the upper layers may be blended together in parallel), **wherein each of the foremost graphics image layer and the corresponding image layers are operatively**

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received from at least one frame buffer (i.e. noted in col. 30 lines 57-59); and a blending module (part of unit 58 in fig. 3) operably coupled to the plurality of video graphics pipelines, (MacInnis at col. 45 lines 7-13 teaches in the preferred embodiment), wherein the blending module is operable to blend the corresponding image layers in a predetermined blending order, thereby creating an intermediate blended image (i.e. noted in col. 44 line 35), and blending the intermediate blended image with the foremost graphics image layer (i.e. noted in col. 44 line 35), to produce an output image having the foremost graphics image layer blended in a foremost position with respect to the other corresponding image layers with negligible loss (MacInnis at col. 50 lines 20-23 teaches read and write cycle simultaneously) of information of the other corresponding image layers, wherein the blending module is selectably controllable to blend the intermediate blended image with the foremost graphics image layer (i.e. noted in col. 46 lines 1-2) in accordance with an alpha blending convention (i.e. noted in col. 46 lines 1-11), also see in col. 32 lines 30-39, or an AND/XOR blending convention (i.e. inherent because in col. 50 lines 11-29 teaches the operation described in the patent is implemented digitally using conventional ASCII technology).. MacInnis at col. 45 lines 7-13 teaches all of the layers that are to be filtered (referred to as "upper" layers) are blended together from back to front using a partial blending operation. In an alternate embodiment, two or more of the upper layers may be blended together in parallel.

MacInnis in col. 13, lines 45-54 discloses that a graphics window with a window layer parameter of 0000b is defined as the bottom most layer, and a graphics window with a window layer parameter of 1111b is defined as the top most layer. MacInnis in col. 44, lines 31-35 discloses that In general, during blending of different layers of graphics and/or video, every

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layer [L1, L2, L33 . . . Ln], where L1 is the back-most layer, each layer is blended with the composition of all of the layers behind it, beginning with L2 being blended on top of L1.

***Examiner's suggestions:** Applicant may emphasize more about the operation in claim 1 lines 13-14 "negligible loss of information", and how does the blending module control the alpha blending with the graphics image layer?*

2. Claims 2, and 4

MacInnis in col. 14 lines 26-37 teaches the graphics blender in fig. 10 #140 as the blending module that determined the alpha value for each pixel, e.g., if the window alpha value is 0.5 on a scale of 0 to 1, coded as 0.x.80, then the effective alpha value of every pixel in the window is one-half of the value encoded in or for the pixel itself. XOR means exclusive or. 'A xor B' means 'A or B, but not both. MacInnis inherently teaches the logical operators, e.g., at col. 14 lines 9-14 teaches the alpha for a pixel is either "0" or "1" not both. AND is another logical operator that returns a true value only if both operands are true that can be easily integrated with XOR.

3. Claims 3 and 14.

Claims 3 and 14 "wherein the blending module is operable to blend the corresponding image layers using alpha blending and a specified per pixel alpha value or a global alpha value, wherein the alpha blending is performed using one of a plurality of pixel depths", MacInnis in col. 5, lines 2-5 discloses image pixel format, pixel color type, alpha blend factor, location on the screen, address in memory, depth order on the screen, or other parameters. The system preferably supports a wide variety of pixel formats, including RGB 16, RGB 15, YUV 4:2:2 (ITU-R 601), CLUT2, CLUT4, CLUT8 or others. In addition to each window having its own

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alpha blend factor, each pixel in the preferred embodiment has its own alpha value. (Definition of alpha blending is: it combines a transparent source color with a translucent destination color.) MacInnis in col. 11 lines 9-20 discloses that often in the creation of graphics displays, the artist or application developer has a need to include rectangular objects on the screen, with the objects having a solid color and a uniform alpha blend factor (alpha value). These regions (or objects) may be rendered with other displayed objects on top of them or beneath them. In conventional graphics devices, such solid color objects are rendered using the number of distinct pixels required to fill the region.

4. Claim 16.

Claim 16 is rejected with similar reason as set forth in claim 1, above.

5. Claim 6.

As for claim 6, "The video graphics module of claim 1, wherein the blending module further comprises a first mixing module and a second mixing module, wherein the first mixing module is operable to blend at least two of the corresponding image layers to produce the intermediate blended image, and wherein the second mixing module is operable to blends the foremost graphics image layer with the intermediate blended image", MacInnis in fig. 2 illustrates mixing modules number 52 (considered as a first mixing module as applicant claimed in the present invention). The video scaler mixing digital, analog and bypass video in, and also outputted to video compositor number 60 (considered as a second mixing module as applicant claimed in the present invention). In fig. 2 a line labeled with "pass through" connecting the three signals from mux (multiplexer) into box 60.

6. Claims 7-8

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Claims 7-8 are rejected with similar reasons as set forth in claims 1 and 3, above.

7. Claim 9

MacInnis in col. 5, lines 2-5 discloses image pixel format, pixel color type, alpha blend factor, location on the screen, address in memory, depth order on the screen, or other parameters. The system preferably supports a wide variety of pixel formats, including RGB 16, RGB 15, YUV 4:2:2 (ITU-R 601), CLUT2, CLUT4, CLUT8 or others. In addition to each window having its own alpha blend factor, each pixel in the preferred embodiment has its own alpha value.

8. Claim 10.

MacInnis in col. 1 lines 54-60 discloses that both the functionality of the graphics and video are common to both. Graphics as used herein may include graphics, text, and video. MacInnis in col. 32 lines 17-29 discloses that The various foreground colors are processed using a low-pass filter as described earlier, and the outline of the entire graphical element (including all colors other than the background) is separately filtered also using a low pass filter as described. The filtered foreground color is used as either the direct color value in, e.g., an alpha RGB format (or other color space, such as alpha YUV) or as the color choice in a CLUT format, and the result of filtering the outline is used as the alpha per pixel value in either a direct color format such as alpha RGB or as the choice of alpha value per CLUT entry in a CLUT format.

9. Claim 11.

See rejection of claim 9, and MacInnis in col. 24 lines 49-52 discloses that For every CLUT-format pixel converted, the pixel data may be used as the address to the CLUT and the resulting value may be used by the converter to produce the YUVa (or alternatively RGBa) pixel value.

10. Claim 12.

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As for claim 12, “A video graphics module comprises: a video graphics pipeline module operable to process at least one image layer; a hardware cursor pipeline operable to process a cursor image; wherein the at least one image layer and the cursor image are operably received from a frame buffer; and a blending circuit operably coupled to the video graphics pipeline and the hardware cursor pipeline operable to process a cursor image (MacInnis in col. 4 line 59 teaches the claimed limitation); wherein the blending circuit is operable to blend, in accordance with an alpha blending convention, the at least one image layer and the cursor image to produce an output image having the cursor image alpha blended in a foremost position with respect to the at least one corresponding image layer”, See rejection of claim 1.

11. Claims 17 and 19-20.

Claims 17 and 19-20, MacInnis in fig. 2 illustrates mixing modules number 52 (considered as a first mixing module as applicant claimed in the present invention). The video scaler mixing digital, analog and bypass video in, and also outputted to video compositor number 60 (considered as a second mixing module as applicant claimed in the present invention). In fig. 2 a line labeled with “pass through” connecting the three signals from mux (multiplexer) into box 60.

12. Claim 18.

MacInnis in cols. 4 and 5 lines 62-67; 1-9 discloses that Graphics windows are preferably characterized by window descriptors. Window descriptors are data structures that describe one or more parameters of the graphics window. Window descriptors may include, for example, image pixel format, pixel color type, alpha blend factor, location on the screen, address in memory, depth order on the screen, or other parameters. The system preferably supports a wide variety of

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pixel formats, including RGB 16, RGB 15, YUV 4:2:2 (ITU-R 601), CLUT2, CLUT4, CLUT8 or others. In addition to each window having its own alpha blend factor, each pixel in the preferred embodiment has its own alpha value. In the preferred embodiment, window descriptors are not used for video windows. Instead, parameters for video windows, such as memory start address and window size are stored in registers associated with the video compositor.

13. Claim 21

MacInnis in fig. 5 box with dashed line labeled number 58, and also shown clearly in fig. 10 the RGB color and the YUV color.

14. Claim 23.

MacInnis in col. 10 lines 4-11 discloses that analog video or MPEG video may be provided to the video compositor as pass through video. Alternatively, either type of video may be captured into memory and provided to the video compositor as a scaled video window. The digitized analog video signals preferably have a pixel sample rate of 13.5 MHz, contain a 16 bit data stream in YUV 4:2:2 format, and include timing signals such as top field and vertical sync signals.

15. Claim 25.

As for claim 25 "The apparatus of claim 33, wherein the memory further comprises operational instructions that cause the processing module to, when the alpha blending mode indicates using the global alpha blending value, retrieve at least one global alpha value from a general alpha register", MacInnis in cols. 4 and 5 lines 62-67; 1-9 discloses that Graphics windows are preferably characterized by window descriptors. Window descriptors are data structures that describe one or more parameters of the graphics window. Window descriptors may include, for

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example, image pixel format, pixel color type, alpha blend factor, location on the screen, address in memory, depth order on the screen, or other parameters. The system preferably supports a wide variety of pixel formats, including RGB 16, RGB 15, YUV 4:2:2 (ITU-R 601), CLUT2, CLUT4, CLUT8 or others. In addition to each window having its own alpha blend factor, each pixel in the preferred embodiment has its own alpha value. In the preferred embodiment, window descriptors are not used for video windows. Instead, parameters for video windows, such as memory start address and window size are stored in registers associated with the video compositor.

16. Claim 26.

As for claim 26, "The apparatus of claim 33, wherein the memory further comprises operational instructions that cause the processing module to, when the alpha blending mode indicates using a per pixel alpha blending value, retrieve at least one corresponding per pixel alpha blending value from an image layer input", MacInnis col. 5 lines 3-9 discloses that in addition to each window having its own alpha blend factor, each pixel in the preferred embodiment has its own alpha value. In the preferred embodiment, window descriptors are not used for video windows. Instead, parameters for video windows, such as memory start address and window size are stored in registers associated with the video compositor.

17. Claim 27.

As for claim 27, "The apparatus of claim 33, wherein the memory further comprises operational instructions that cause the processing module to, when the alpha blending mode indicates using the key alpha blending value, retrieve an alpha key indication from a keyer, wherein the keyer generates the alpha key indication from at least one corresponding per pixel alpha value

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associated with an image layer input”, MacInnis at col. 14 lines 9-14 teaches “a chroma keying” that is similar to what the claimed invention recited. MacInnis in col. 14 lines 1-6 discloses that the alpha type of 00b indicates that the alpha value is to be selected from chroma keying.

Chroma keying determines whether each pixel is opaque or transparent based on the color of the pixel.

18. Claim 28.

Claim 28 is rejected with similar reason as set forth in claims 1, 25-27, above.

19. Claim 29.

As for claim 29, MacInnis at col. 14 lines 9-14 teaches “a chroma keying” that is similar to what the claimed invention recited. MacInnis in col. 14 lines 1-6 discloses that the alpha type of 00b indicates that the alpha value is to be selected from chroma keying. Chroma keying determines whether each pixel is opaque or transparent based on the color of the pixel.

20. Claim 30.

As for claim 30, MacInnis in fig. 28 a flow diagram of a process of blending video and graphics surfaces is illustrated. The graphics display system resets in step 902. In step 904, the video compositor blends the pass through video and the background color with the scaled video window, using the alpha value, which is associated with the scaled video window. The result of this blending operation is then blended with the output of the graphics display pipeline. The graphics output has been pre-blended in the graphics blender in step 904 and filtered in step 906, and blended graphics contain the correct alpha value for multiplication by the video output. The output of the video blend function is multiplied by the video alpha, which is obtained from the

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graphics pipeline, and the resulting video and graphics pixel data stream are added together to produce the final blended result .

21. Claim 31.

As for claim 31, MacInnis in fig. 5 illustrates a plurality of multiplexer MUX 162, MUX 168, MUX 176 and MUX 188.

22. Claim 32.

As for claim 32, MacInnis in fig. 5 illustrates the limitation of outputting image layers.

23. Claim 33.

Claim 33 is rejected with similar reason as set forth in claim 1, above.

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Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javid A. Amini whose telephone number is 571-272-7654. The examiner can normally be reached on 8-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Javid A Amini
Examiner
Art Unit 2628

J.A.



KEE M. TUNG
SUPERVISORY PATENT EXAMINER